REMARKS

Reconsideration of this application is respectfully requested.

Claims 1-7 are pending in the application, with Claims 1 and 5 being the independent claims. Claims 1 and 5-7 are rejected under 35 U.S.C. §102(b) as being anticipated by Khlat (E.P. 0948128 A1). Claim 2 is rejected under 35 U.S.C. §103(a) as being unpatentable over Khlat in view of Adachi (US 2002/0155822 A1) in further view of Kataoka et al. (JP 10247953). Claim 4 is rejected under 35 U.S.C. §103(a) as being unpatentable over Khlat in view of Mitama (EP 0863606A1). Claim 3 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all limitations of the base claim and any intervening claims.

It is respectfully submitted that the Examiner is incorrect in rejecting Claims 1, 5-7 under 35 U.S.C. §102(b) based on *Khlat*. *Khlat* neither discloses nor suggests each and every element of independent Claims 1 and 5, and thus it does not anticipate the claims.

Claim 1 utilizes "means for" recitations, and as such requires the Examiner to consider the specific structure described in the specification to interpret these limitations. In particular, Claim 1 recites a direct-conversion receiver for substantially removing DC offset signals in a mobile communication terminal wherein the receiver comprises, in part an adjusting means for substantially reducing the difference. Khlat, as cited by the Examiner, takes the output from a low pass filter and subtracts the outputs; thereby providing a means for reducing the difference between the two DC offset components, but does not teach or suggest the specific structure disclosed by the invention, namely the feedback loop circuit 600c. Khlat instead discloses that the gain/phase correction block 200 may be realized in hardware or software. However, Khlat disclosed a hardware implementation shown in Fig. 2 consisting of a gain adjustment & phase θ correction 200 and complex low pass filter 210. Khlat discloses that the Ad and θ control signals are factory set, and are intended to remove any phase or gain mismatches occurring between

the I and Q paths as a result of analog device variations. The Iout and Qout signals are then filtered by the complex LPF 210 to produce IDCest and QDCest signals representing the DC offset component of the Iout and Qout signals.

In contrast, the feedback loop circuit disclosed by the present invention includes a high gain amplifier 623 for detecting the DC offset component, an analog-to-digital converter (ADC) 621 for transforming an analog DC offset signal to a digital signal to enable a digital signal processor (DSP) 619 to read the signal and determine whether the DC offset is zero or not and output a pertinent voltage control voltage to an automatic gain controller to adjust the DC offset signal to zero. The present invention, as claimed, does not read on Khlat because the two implementations differ diametrically. Therefore, the "means for" limitation recited in the invention cannot be broadly interpreted by the Examiner to read on the implementation taught by Khlat. In re Donaldson Co., 16 F.3d 1189, 29 USPQ2d 1845 (Fed. Cir. 1994). The structure disclosed by the Applicant cannot be disregarded. Because Khlat does not teach or suggest each and every element of Claim 1, it does not anticipate Claim 1. Furthermore, Claim 1 has been amended to recite "determining whether the DC offset is zero and outputting a control voltage to adjust the DC offset signal to zero" which is not disclosed by Khlat.

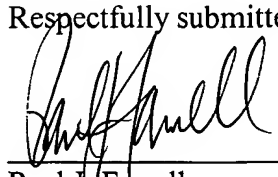
Claims 2-4 depend from and contain all the elements of Claim 1. Claims 2-4 are distinguishable from Khlat in the same manner as Claim 1. Furthermore, in rejecting Claim 2 the Examiner failed to articulate a proper motivation. Instead, the Examiner indicated the result of modifying Khlat by the teachings of (a) Adachi producing one of the methods among many possible methods to generate I and Q components and (b) Kataoka producing the means for fine tuning DC offset cancellation in the receiver. The Examiner articulates the result of modifying the references but fails to explicate why an artisan of ordinary skill in the art would be motivated to perform said modifications. Therefore, should this Response not place the application into condition for allowance, another non-Final Action is respectfully requested.

Moreover, in rejecting Claim 4 the motivation as articulated by the Examiner is hopelessly deficient. The Examiner asserted: "Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Adachi's system to provide for the following: a switching means for connecting the converting means to detecting means as this arrangement would provide alternative method for implementing DC offset cancellation in a receiver as taught by Mitama." Once again, the Examiner articulates the result of modifying the reference but fails to explicate why an artisan of ordinary skill in the art would be motivated to perform said modifications. This is another reason why a non-Final Action should be granted.

The Examiner alleges that Khlat discloses the method of Claim 5. However, Khlat fails to disclose " determining whether the DC offset is zero and outputting a control voltage to adjust the DC offset signal to zero." As a result, Khlat fails to teach or suggest each and every element of Applicants' Claim 5 as amended. Thus, Khlat fails to anticipate Claim 5 as amended.

The application as now presented, containing Claims 1-7 are believed to be in condition for allowance. Should the Examiner believe that a telephone conference or personal interview would facilitate resolution of any remaining matters, the Examiner may contact Applicant's attorney at the number given below.

Respectfully submitted,



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